

DESCRIPTION

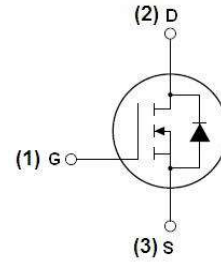
The 30N06 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

GENERAL FEATURES

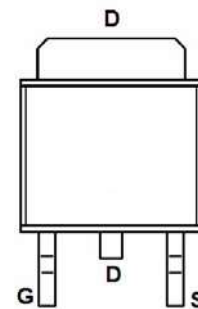
- | V_{DSS} | $R_{DS(ON)}$
@ 10V (typ) | I_D |
|-----------|-----------------------------|-------|
| 60V | 26 m Ω | 30 A |
- High density cell design for ultra low R_{dson}
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

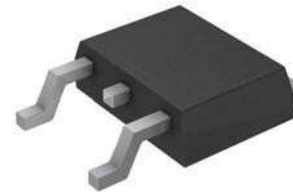
- Power switching application
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply



Schematic diagram



Marking and pin Assignment



TO-252

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	30	A
Drain Current-Continuous($T_C=100^\circ\text{C}$)	$I_D(100^\circ\text{C})$	17	A
Pulsed Drain Current	I_{DM}	75	A
Maximum Power Dissipation	P_D	50	W
Derating factor		0.33	W/°C
Single pulse avalanche energy (Note 5)	E_{AS}	110	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	°C

Thermal Characteristic

Thermal Resistance, Junction-to-Case(Note 2)	$R_{\theta JC}$	3.0	°C/W
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Electrical Characteristics (TA=25°C unless otherwise noted)

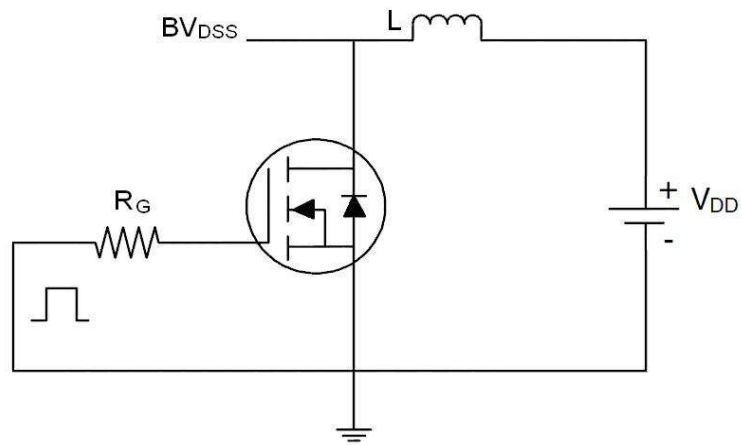
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	60	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=60V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	-	3.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=15A$	-	26	30	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=4.5A$	11	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{iss}	$V_{DS}=30V, V_{GS}=0V,$ $F=1.0MHz$	-	1890	-	PF
Output Capacitance	C_{oss}		-	168	-	PF
Reverse Transfer Capacitance	C_{rss}		-	132	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=30V, I_D=2A, R_L=6.7\Omega$ $V_{GS}=10V, R_G=3\Omega$	-	7	-	nS
Turn-on Rise Time	t_r		-	3.2	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	19.2	-	nS
Turn-Off Fall Time	t_f		-	3.2	-	nS
Total Gate Charge	Q_g	$V_{DS}=48V, I_D=10A,$ $V_{GS}=10V$	-	49	-	nC
Gate-Source Charge	Q_{gs}		-	8	-	nC
Gate-Drain Charge	Q_{gd}		-	16	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=10A$	-	-	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	25	A
Reverse Recovery Time	t_{rr}	$T_J = 25^\circ C, I_F = 10A$	-	35	-	nS
Reverse Recovery Charge	Q_{rr}	$di/dt = 100A/\mu s$ (Note3)	-	43	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

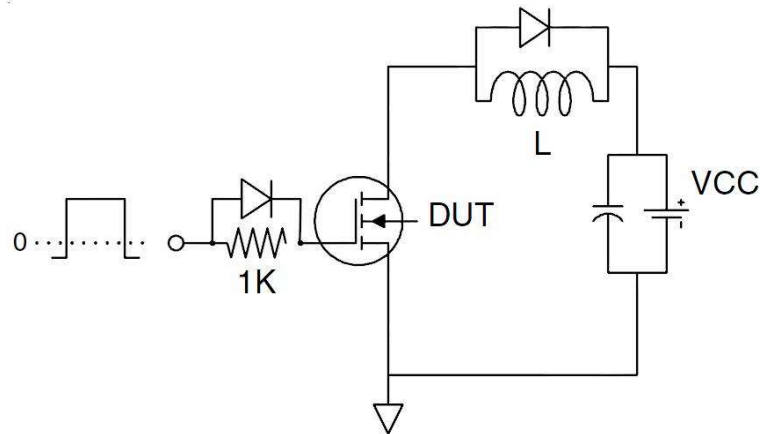
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition : $T_J=25^\circ C, V_{DD}=30V, V_G=10V, L=0.5mH, R_g=25\Omega$

Test circuit

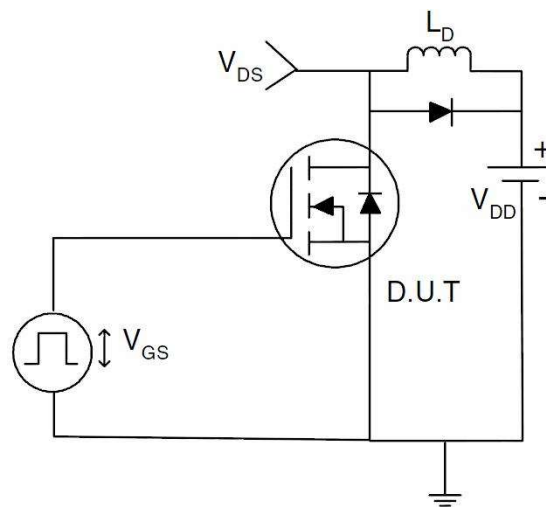
1) E_{AS} test Circuits



2) Gate charge test Circuit:



3) Switch Time Test Circuit:



N-Channel Enhancement Mode Power MOSFET

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (Curves)

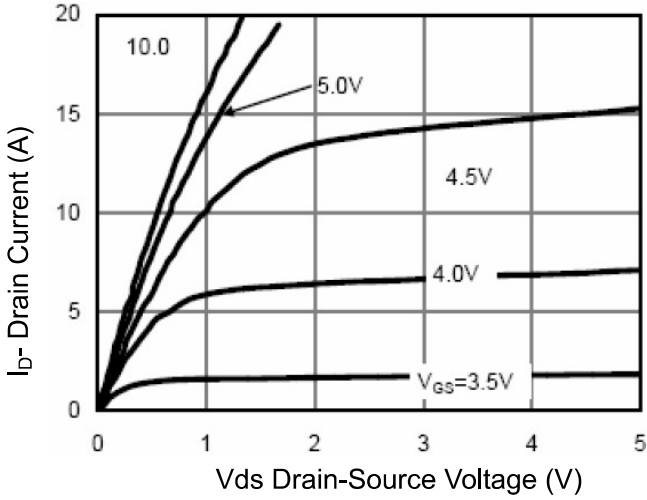


Figure 1 Output Characteristics

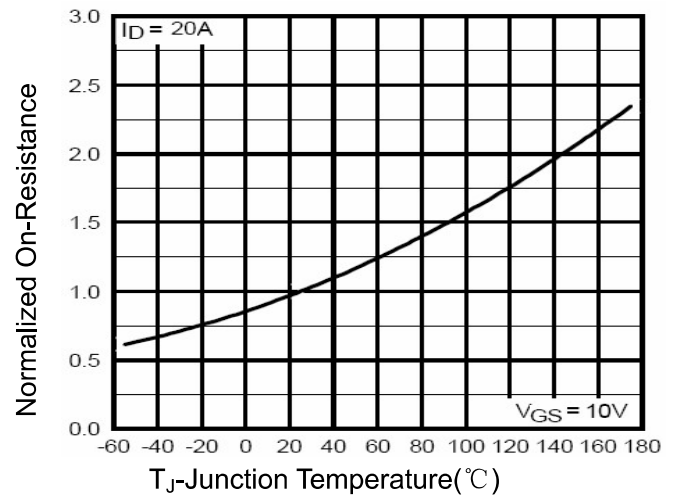


Figure 4 Rdson-Junction Temperature

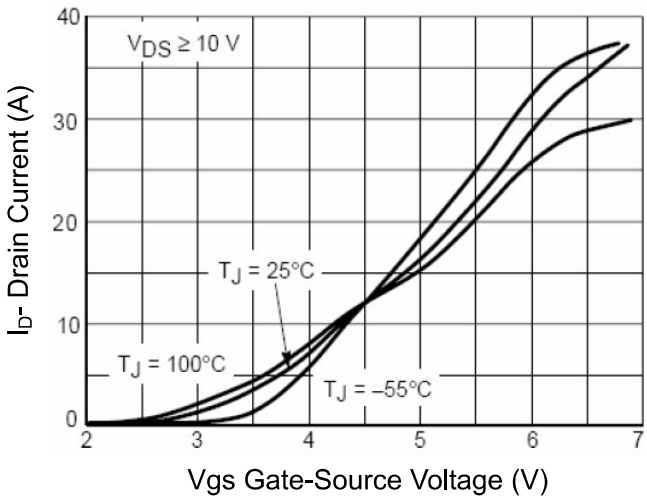


Figure 2 Transfer Characteristics

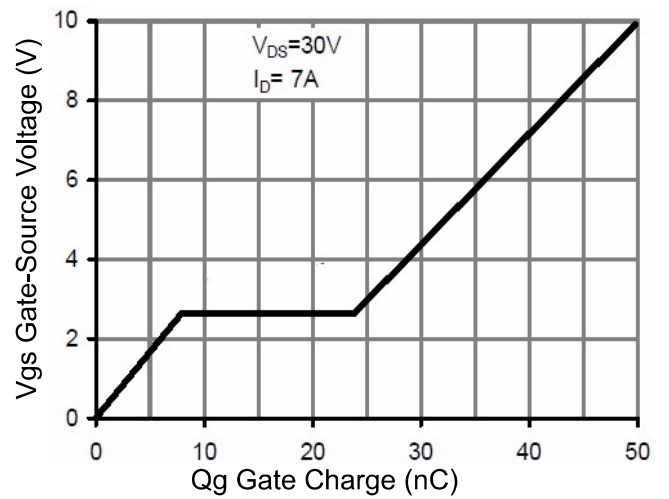


Figure 5 Gate Charge

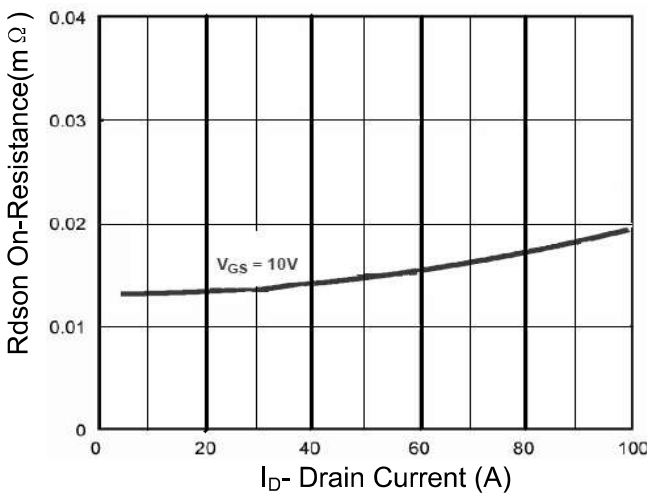


Figure 3 Rdson- Drain Current

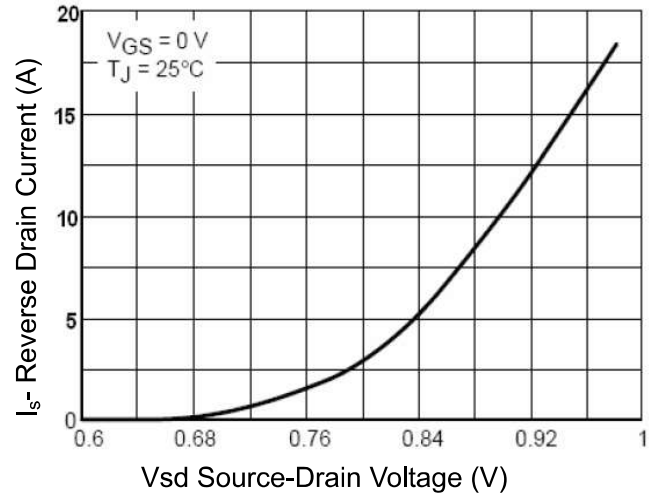


Figure 6 Source- Drain Diode Forward

N-Channel Enhancement Mode Power MOSFET

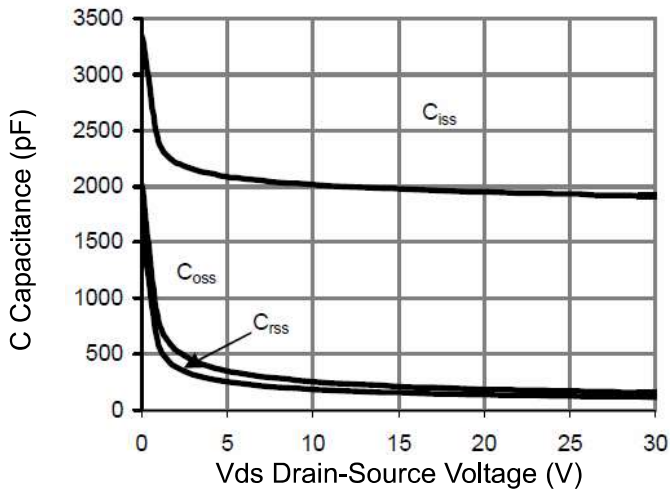


Figure 7 Capacitance vs Vds

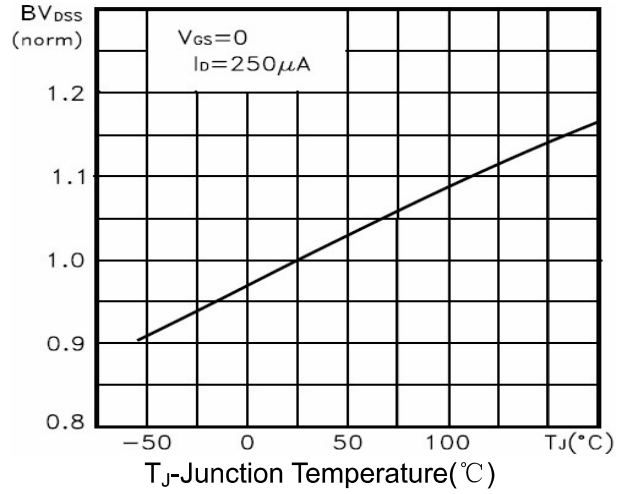


Figure 9 BV_{DSS} vs Junction Temperature

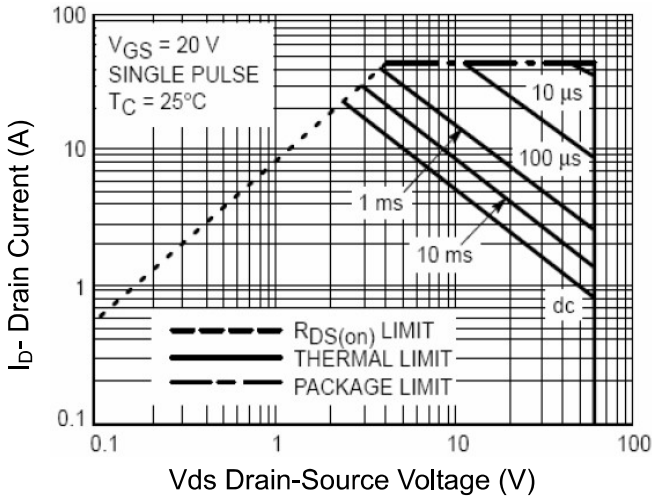


Figure 8 Safe Operation Area

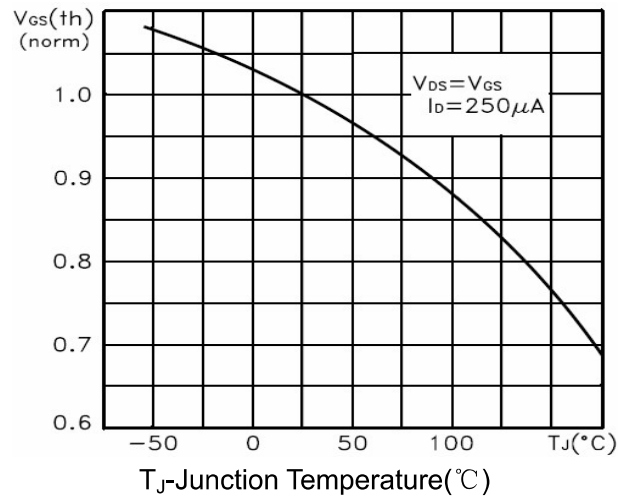


Figure 10 $V_{GS(th)}$ vs Junction Temperature

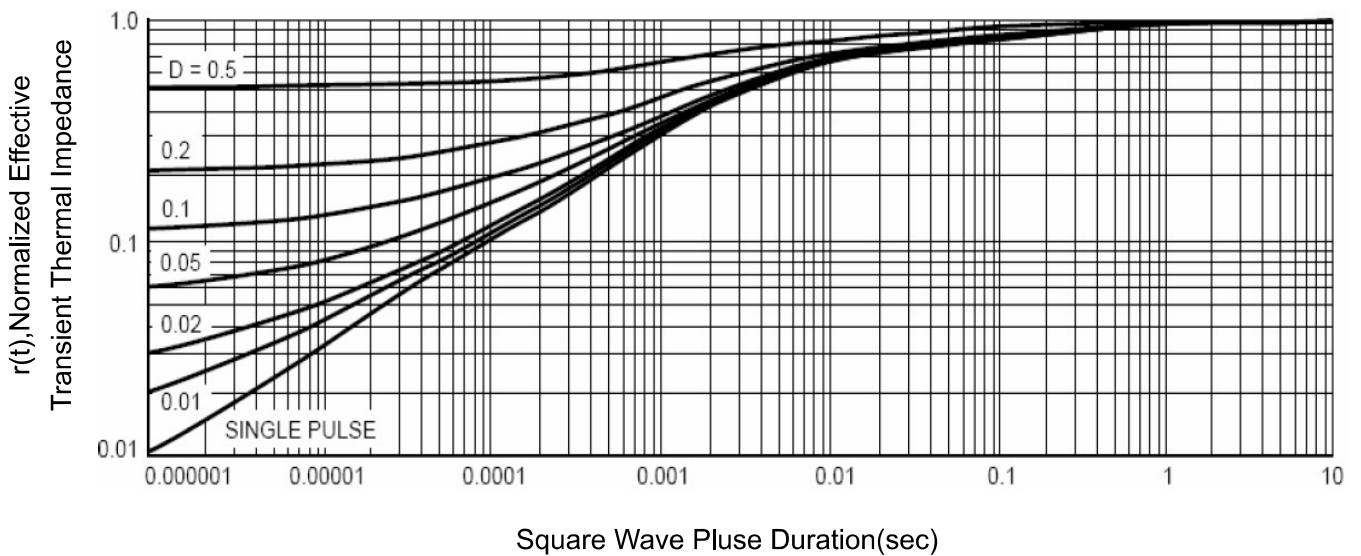


Figure 11 Normalized Maximum Transient Thermal Impedance